What is claimed is:

1) A method, comprising the steps of:

initializing a system parameter;

operating a processing device responsive to the system parameter;

obtaining an operational value;

comparing the operational value to a threshold value; and,

adjusting the system parameter responsive to the comparing step.

2) The method of claim 1, wherein the system parameter is a page closing time stored in a memory controller.

3) The method of claim 2, wherein the obtaining step includes determining a difference between page hits and page misses during a period of time.

4) The method of claim 3, wherein the obtaining step is performed by a first counter capable to obtain a number of page hits and a second counter capable to obtain a number of page misses and comparator logic capable to output a parameter adjust signal responsive to the difference and the threshold value.

5) The method of claim 1, wherein the initializing step is performed by a BIOS software component.

6) The method of claim 1, wherein the system parameter is a processor operating frequency.

7) The method of claim 1, wherein the system parameter is the number of memory devices in a memory module operating in a particular mode of operation.

8) A method, comprising the steps of:

counting a number of page hits during a period of time;

counting a number of page misses during the period of time;

comparing the number of page hits to the number of page misses; and,

adjusting a page closing time value responsive to the comparing step.

9) The method of claim 8, wherein the adjusting step includes:

increasing the page closing time value responsive to the comparing step.

10) The method of claim 8, wherein the adjusting step includes:

decreasing the page closing time value responsive to the comparing step.

11) The method of claim 8, wherein the number of page hits is greater than the number of page misses.

12) The method of claim 8, wherein the number of page hits is less than the number of page misses.

13) A device, comprising:

a first counter capable to output a number of page misses during a period of time;

a second counter capable to output a number of page hits during the period of time; and,

a comparator logic, coupled to the first and second counters, capable to output an adjust signal responsive to a comparison of a difference between the number of page hits and page misses to a threshold value.

14) The device of claim 13, wherein the adjust signal increments a page closing time value.

15) The device of claim 13, wherein the adjust signal decrements a page closing time value.

16) The device of claim 13, wherein an average memory access time ("AMAT") is decreased.

17) The device of claim 13, wherein power consumption is decreased.

18) The device of claim 13, wherein a BIOS software component initializes the period of time and the threshold value.

19) The device of claim 13, wherein the adjust signal adjusts a page closing time value stored in the memory controller.

20) The device of claim 13, wherein the device is a memory controller.

21) The device of claim 13, wherein the device is coupled to a memory module.

22) An apparatus, comprising:

a master device capable to retrieve data responsive to a page close time value, including,

a first counter capable to output a number of page misses during a period of time;

a second counter capable to output a number of page hits during the period of time;

a comparator logic, coupled to the first and second counters, capable to output an adjust signal responsive to a comparison of a difference between the number of page hits and page misses to a threshold value, wherein the adjust signal adjusts the page close time value; and,

a memory device, coupled to the master device, to provide the data.

23) The apparatus of claim 22, wherein the threshold value and the period of time is initialized by a BIOS software component.

24) The apparatus of claim 22, wherein the master device is a memory controller.

25) The apparatus of claim 22, wherein the master device is a processor.

26) The apparatus of claim 22, wherein the memory device is a Dynamic Random Access Memory ("DRAM") device.

27) The apparatus of claim 22, wherein the memory device is included in a memory module.

28) An article of manufacture, including a processor readable medium, comprising:

a first software component capable to initialize a system parameter;

a second software component capable of obtaining an operational value; and,

a third software component capable of adjusting the system parameter responsive to the operational value.

29) A device, comprising:

a memory capable of storing a page closing time value; and,

means for adjusting the page closing time value responsive to an operational value.